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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Application No.: 10/045,137 Confirmation No.: 3416  
First Named Inventor: Wang, Albert Z. H. Filing Date: 23 October 2001  
Group Art Unit: 2811 Examiner: Hu, S.  
Atty. Docket No.: NS-3868-2C US  
Title: Dual Direction Over-Voltage And Over-Current IC Protection  
Device And Its Cell Structure  
Assignee(s): National Semiconductor Corporation

Mountain View, California  
8 January 2004

**COMMISSIONER FOR PATENTS**  
**PO Box 1450**  
**Alexandria, Virginia 22313-1450**

**INFORMATION DISCLOSURE STATEMENT**  
**UNDER 37 CFR 1.97(c) WITH FEE UNDER 37 CFR 1.17(p)**

Sir:

Pursuant to 37 CFR 1.56, 1.97, and 1.98, each document listed on the accompanying substitute PTO Form 1449 is called to the attention of the Examiner for the above patent application. A copy of each listed document is enclosed.

Gray et al. was cited in the Amendment submitted 10 June 2003 for revising the text of the present application.

Citation of each listed document shall not be construed as:

1. an admission that the document is necessarily prior art with respect to the instant invention;
2. a representation that a search has been made, other than as described herein;  
or
3. an admission that the information cited herein is, or is considered to be, material to patentability as defined in 37 CFR 1.56(b).

Ronald J. Meetin  
Attorney at Law  
210 Central Avenue  
Mountain View, CA  
94043-4869  
Tel.: 650-964-9767  
Fax: 650-964-9779

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This information disclosure statement is submitted under the provisions of 37 CFR 1.97(c). Please charge the information disclosure statement fee of \$180 as set forth in 37 CFR 1.17(p) to Deposit Account 502641. This paper is being submitted in duplicate.

**EXPRESS MAIL LABEL NO.:**

**EV 337 116 190 US**

Respectfully submitted,

*Ronald J. Meetin*

Ronald J. Meetin  
Attorney for Applicant(s)  
Reg. No. 29,089

210 Central Avenue  
Mountain View, CA 94043-4869

Ronald J. Meetin  
Attorney at Law  
210 Central Avenue  
Mountain View, CA  
94043-4869

Tel.: 650-964-9767  
Fax: 650-964-9779

U.S. Department of Commerce, Patent and Trademark Office				Atty Docket No.		Application No.	
				NS-3868-2C US		10/045,137	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Applicant(s)		Confirmation No.	
Substitute Form PTO 1449				Wang, Albert Z. H.		3416	
				Filing Date		Group	
				23 October 2001		2811	

  

U.S. Patent Documents							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	3,140,963	07/1964	Svedberg et al.	148	33.5	
	AB	3,427,512	02/1969	Mapother	257	162	
	AC	3,904,931	09/1975	Leidich	317	016	
	AD	4,400,711	08/1983	Avery	357	043	
	AE	4,484,244	11/1984	Avery	361	056	
	AF	4,543,593	09/1985	Fujita	357	048	
	AG	4,567,500	01/1986	Avery	357	038	
	AH	4,581,626	04/1986	Krishna et al.	257	164	
	AI	4,595,941	06/1987	Avery	357	043	
	AJ	4,633,283	12/1986	Avery	357	023	
	AK	4,870,530	09/1989	Hurst et al.	361	091	
	AL	4,967,256	10/1990	Pathak et al.	257	112	
	AM	5,140,401	08/1992	Ker et al.	357	43	

  

Foreign Patent Documents							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
	AN							
	AO							
	AP							
	AQ							
	AR							

  

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)	
AS	Gray et al, <u>Analysis and Design of Analog Integrated Circuits</u> (John Wiley & Sons), 1997, pps. 197 - 210
AT	
AU	

  

Examiner	Date Considered
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\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

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U.S. Patent Documents								
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
	BA	5,359,211	10/1994	Croft	257	173		
	BB	5,400,202	03/1995	Metz et al.	361	56		
	BC	5,430,595	07/1995	Wagner et al.	361	56		
	BD	5,455,436	10/1995	Cheng	257	356		
	BE	5,465,189	11/1995	Polgreen et al.	361	58		
	BF	5,561,577	10/1996	Motley	361	56		
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	BJ	5,600,525	02/1997	Avery	361	56		
	BK	5,793,066	08/1998	Ajit	257	152		
	BL	5,808,326	09/1998	Bernier, et al.	257	109		
	BM							
Foreign Patent Documents								
							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
	BN							
	BO							
	BP							
	BQ							
	BR							
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)								
	BS							
	BT							
	BU							
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